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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,182	MICHELONI ET AL.	
	Examiner	Art Unit	
	Matt Urick	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Non-Final Official Action

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in The European Patent Office on 3/19/03. It is noted, however, that applicant has not filed a certified copy of the 03425171.0 application as required by 35 U.S.C. 119(b).

Claim Objections

Claims 2 and 5 are objected to due to the following informalities: Claims 2 and 5 contain the limitation "said means," and both claims contain "means of an interface bus" and "circuit means." Based on the context of the claim language, the term "said means" is assumed to refer to the term "circuit means." Appropriate correction is required.

Claim 3 recites the limitation "the syndrome" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 3 is objected to due to the following informalities: Claim 3 contains the limitation "...the memory said means comprise:" which is taken to mean "~~the memory~~ said means comprise:" Appropriate correction is required.

Claim 6 recites the limitation "said coding block" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the coding block" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the parity calculation circuit" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 contains the limitation "...logic for calculating the syndrome uses again the parity calculation circuit of the coding block." A parity calculation circuit is not claimed before this step, so it is not clear when the parity calculation circuit was used for the first time. Additionally, there is a lack of antecedent basis for the limitations "parity calculation circuit" and "coding block."

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5, 9, 10, 12-14, 17, and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Pittelkow (US Patent 6,996,741).

As per claim 1, Pittelkow discloses:

An integrated memory system (figure 2: controller 201), comprising at least a non-volatile memory (figure 2: NVRAM 228 is non volatile, and interfaces 222a-222c lead to disk storage, which is nonvolatile; column 8 lines 36-43: configuration control board 202 may also contain NVRAM), and an automatic storage error corrector (column 9 lines 36-43), characterized in that the memory system comprises circuit means, functionally independent (figure 5: multiple independent configuration circuit boards may be used),

each of them being responsible for the correction of a predetermined storage error (column 25: table lists predetermined error types);

at least one of said means generating a signal to ask a correction being external to the memory (column 9 lines 36-40: the CCB may send the failure to another failure manager which may be in another controller. The limitation: "external to the memory" is taken to mean: "external to the non-volatile memory," as opposed to "external to the memory system").

As per claim 2, Pittelkow discloses:

A system according to claim 1, characterized in that said memory is connected to a controller by means of an interface bus (column 8 lines 36-43: configuration control board 202 may contain NVRAM: this would require a bus for access. Figure 2: NVRAM

is accessed by front and back end processors, which are connected to CCB by busses 214 and 218. Disk storage is connected by bus 226 (also figure 2)).

and said means are incorporated both in the memory and in the controller (figure 2: configuration control board is incorporated with the nonvolatile memories).

As per claim 5, Pittelkow discloses:

A system according to claim 2, characterized in that said means comprise a circuit for generating a signal activated to request the external correction of an error by said controller (column 9 lines 36-40: the CCB may send the failure to another failure manager, which may be in another controller).

As per claim 9, Pittelkow discloses:

A system, comprising:

a first circuit operable to store data having associated therewith at least one storage error of a plurality of storage-error types the first circuit operable to correct a first-type error of the plurality of storage-error types (figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25); and

a second circuit coupled to the first circuit (figure 5: multiple storage controllers may be used and coupled),

the second circuit operable to correct a second-type error of the plurality of storage-error types (figures 2 and 3: storage controller 201 contains failure manager

302, which is capable of detecting the types of errors listed in the table of column 25).

As per claim 10, Pittelkow discloses:

The system of claim 9 wherein the second circuit is operable to generate a signal requesting correction of a third-type error of the plurality of storage-error types (column 25: several different error types can be detected. Column 9 lines 36-40: the CCB may send the failure to another failure manager which may be in another controller. Column 4 lines 9-13: a master and one or more slave controllers may be used)

As per claim 12, Pittelkow discloses:

The system of claim 9 wherein the first circuit is further operable to detect the second-type error (figures 2 and 3: storage controller 201 contains failure manager 302, which is capable of detecting any of the types of errors listed in the table of column 25).

As per claim 13, Pittelkow discloses:

The system of claim 9 wherein the second circuit corrects the second-type error in response to a signal generated by the first circuit (column 9 lines 36-40: the CCB may send the failure to another failure manager which handles the error).

As per claim 14, Pittelkow discloses:

The system of claim 9 wherein the first circuit comprises a non-volatile memory (figure 2: NVRAM 228 is non volatile, and interface 22a-222c lead to disk storage, which

is nonvolatile; column 8 lines 36-43: configuration control board 202 may also contain NVRAM).

As per claim 17, Pittelkow discloses:

A memory device, comprising:

a storage portion operable to store data having associated therewith at least one storage error of a plurality of storage-error types (column 8 lines 48-53: the CCB is associated with RAID devices, and may perform failure notification and diagnostics on the RAID devices);

a first circuit operable to correct a first-type error of the plurality of storage-error types (figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25); and

a second circuit operable to generate a signal indicating detection of a second-type error of the plurality of storage-error types (figure 5: multiple independent configuration circuit boards may be used).

As per claim 19, Pittelkow discloses:

A method, comprising:

storing, in a memory location of a device, data having associated therewith at least one storage error of a plurality of storage-error (figures 2 and 3, and column 9

lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25); and

correcting, at the memory location, a first-type error of the plurality of storage-error types (figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25).

As per claim 20, Pittelkow discloses:

The method of claim 19, further comprising generating, at the memory location, an interrupt-request signal indicating detection of a second-type error of the plurality of storage-error types (column 9 lines 36-40).

As per claim 21, Pittelkow discloses:

An electronic system, comprising:

a first integrated circuit having a memory operable to store data having associated therewith at least one storage error of a plurality of storage-error types, the memory operable to correct a first-type error of the plurality of storage-error types (figures 2 and 3, and column 9 lines 36-40: storage controller 201 contains failure manager 302, which is capable of detecting and correcting errors such as those listed in the table of column 25); and

a second integrated circuit coupled to the first circuit, the second integrated circuit having processor operable to correct a second-type error of the plurality of

storage-error types (figure 5: multiple independent configuration circuit boards may be used. Column 8 lines 36-43: this may include a processor).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 4, 6-8, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pittelkow (US Patent 6,996,741) in view of Saxena (US 5,533,035).

As per claim 3, Pittelkow does not disclose:

A system according to claim 1, characterized in that in the memory said means comprise:

a circuit for correcting a single error

circuits for the coding required to correct two errors;

a logic for calculating the syndrome;

a logic for detecting more than one error.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data

(column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow, increasing reliability.

As per claim 4, Pittelkow does not disclose:

A system according to claim 3, characterized in that said means also comprise: a logic for bringing to the controller:

a one-or-no-error-corrected data

the uncorrected error; and

the calculated syndrome.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column

10 lines 53-56), or a double bit error (column 10 lines 56-60). These steps are executed in an error correction unit (column 10 lines 21-25). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow, increasing reliability.

As per claim 6, Pittelkow discloses:

A system according to claim 3, characterized in that said coding block is located immediately downstream of the input terminal of said memory and performs a vector product proportional to the number of parity bits and obtained through the synthesis of a corresponding logic function.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). The error correction code is calculated by the synthesis of a series of logic functions (column 7 lines 20-29). These steps are performed by error code generator 30, immediately downstream of the

an input terminal (column 5 lines 38-40 and figure 1) . Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow, increasing reliability.

As per claim 7, Saxena discloses:

A system according to claim 6, characterized in that said logic for calculating the syndrome uses again the parity calculation circuit of the coding block.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). The error correction code is calculated by error code generator 30 (column 5 lines 38-40 and figure 1) . Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple

errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow, increasing reliability.

As per claim 8, Pittelkow discloses:

A system according to claim 3, characterized in that said circuit for correcting a single error comprises a block for decoding a single error effective to recognise each of the several syndromes associated to a single error to activate, through a corresponding vector, the correction of the corresponding bit.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42); and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error

correction capabilities and syndrome calculation into the system of Pittelkow, increasing reliability.

As per claim 11, Pittelkow discloses:

The system of claim 9 wherein the first circuit is further operable to determine at least one syndrome associated with the at least one storage error.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager (column 26 lines 20-27). An error correction code capable of correcting more than one error in a dataset would enable the system to correct multiple errors instead of just one. This would be an obvious benefit in retaining reliability of storage systems, because data with more than 1 bit error would not be lost. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate error correction capabilities and syndrome calculation into the system of Pittelkow, increasing reliability.

As per claim 18, Pittelkow does not disclose:

The device of claim 17, further comprising a third circuit operable to determine at least one syndrome associated with the at least one storage error.

Saxena discloses a system (figure 5) that reads data having error-correction code from a memory (column 10 lines 21-28), calculates a syndrome for the data (column 10 lines 35-42), and, using the syndrome, corrects a single bit error, (column 10 lines 53-56), or a double bit error (column 10 lines 56-60). Pittelkow discloses that an error correction code may be used (column 25 lines 30-34: "Single Bit Error Correction Code Error"), and that other types of errors may also be corrected in the failure manager portion of the controller (column 26 lines 20-27). Pittelkow also discloses that any number of controllers may be used (column 4 lines 9-13: a master and one or more slave controllers). A syndrome calculator would enable the controller to find and correct one or more errors in the ECC data. This would have the obvious benefit of improving reliability of storage systems, because data with more than 1 bit error would be correctable. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate syndrome calculation into the system of Pittelkow, increasing reliability.

Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pittelkow (US Patent 6,996,741) in view of Null (The Essentials of Computer Organization and Architecture).

As per claim 15, Pittelkow does not disclose:

The system of claim 9 wherein: the first circuit is disposed on a first integrated circuit; and the second circuit is disposed on a second integrated circuit.

Pittelkow discloses that his storage controller comprises a plurality of processors, a configuration and control board, and storage means(column 7 lines 39-47). Null discloses that an integrated circuit is a well-known means of integrated up to millions of logic gates and electronic components, and enabling them to interface with outside components (page 106 section 3.4.2). Pittelkow also discloses that the controllers may be separate and connected by a network (figure 5: controller 1 and controller 2 are connected by administrative network 520). Additionally, Null discloses that integrated circuits use little power consumption and take up small amounts of space (page 106 section 3.4.2). Using an integrated circuit would enable the system to take advantage of well-known technology and consume less power and space than constructing each gate and component separately. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate integrated circuits into the system of Pittelkow, consuming less power and space.

As per claim 16, Pittelkow does not disclose:

The system of claim 9 wherein the first and second circuits are disposed on an integrated circuit.

Pittelkow discloses that his storage controller comprises a plurality of processors, a configuration and control board, and storage means(column 7 lines 39-47). Null

discloses that an integrated circuit is a well-known means of integrated up to millions of logic gates and electronic components, and enabling them to interface with outside components (page 106 section 3.4.2). Additionally, Null discloses that integrated circuits use little power consumption and take up small amounts of space (page 106 section 3.4.2). Using an integrated circuit would enable the system to take advantage of well-known technology and consume less power and space than constructing each gate and component separately. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate integrated circuits into the system of Pittelkow, consuming less power and space.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matt Urick whose telephone number is (571) 272-0805. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MTU